This Page Is Inserted by IFW Operations and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (currently amended): A semiconductor device comprising:

a first semiconductor layer formed above a first region of a supporting substrate with a buried oxide layer disposed therebetween, and

a second semiconductor layer formed on a second region of the supporting substrate,
wherein an interface between the supporting substrate and said second
semiconductor layer is placed in a position deeper than the buried oxide layer

a supporting substrate comprising a first region and a second region, the second region of the supporting substrate having a surface lower than a surface of the first region of the supporting substrate;

a buried oxide layer formed above the first region of the supporting substrate;

a semiconductor layer formed above the buried oxide layer; and

an epitaxial layer formed above the second region of the supporting substrate,

an interface between the epitaxial layer and the supporting substrate being set in a

portion which lies deeper than the buried oxide layer.

Claim 2 (Previously Presented): The semiconductor device according to claim 1, wherein an upper surface of said second semiconductor layer is positioned higher than an upper surface of the supporting substrate.

Claim 3 (Currently Amended): The semiconductor device according to claim 1, further comprising a first element formed in said first semiconductor layer, a second element

Application No. 10/078,344

Reply to Office Action of August 8, 2003.

formed in said second semiconductor epitaxial layer, and an active region of said second

element formed to avoid crossing the interface between the supporting substrate and said

second semiconductor epitaxial layer.

Claim 4 (Canceled).

Claim 5 (original): The semiconductor device according to claim 1, wherein the

interface between the supporting substrate and said second semiconductor layer is an

interface of bonding the supporting substrate and said second semiconductor layer.

Claim 6 (Currently Amended): The semiconductor device according to claim 1,

wherein the supporting substrate, said semiconductor layer and said epitaxial layer and said

first and second semiconductor layers are formed of silicon and the buried oxide layer is

formed of silicon oxide.

Claim 7 (Previously Presented): The semiconductor device according to claim 1,

wherein a concentration of oxygen in a portion of the supporting substrate which lies near the

interface between the supporting substrate and said second semiconductor layer is lower than

a concentration of oxygen in a portion of the supporting substrate which lies near and directly

under the buried oxide layer.

Claim 8 (Canceled).

3

Claim 9 (Currently Amended): The semiconductor device according to claim 3, wherein said second element includes a trench type memory cell of a DRAM and the interface between the supporting substrate and said second semiconductor epitaxial layer is set in a portion which lies deeper than the buried oxide layer and crosses a trench capacitor of the trench type memory cell.

Claims 10-25 (canceled).

Claim 26 (New): A semiconductor device comprising:

a first semiconductor layer formed above a first region of a supporting substrate with a buried oxide layer disposed therebetween;

a first element formed in the first semiconductor layer;

a second semiconductor layer formed above a second region of the supporting substrate; and

a second element formed in the second semiconductor layer, the second element including a trench type memory cell of a DRAM, and a trench capacitor of the trench type memory cell crossing an interface between the supporting substrate and the second semiconductor layer,

the interface between the supporting substrate and the second semiconductor layer being set in a portion which lies deeper than the buried oxide layer.